



# DP637 Embedded DisplayPort™ Timing Controller

## For High Pixel Density Mobile Displays

Product Brief

**DP637**

### FEATURES

- Supports display resolutions exceeding 2560x1600
- Compliant to VESA Embedded DisplayPort version 1.2
- Includes eDP v1.2 backlight control through AUX
- 1.62 and 2.7Gbps eDP link operation with 1, 2, or 4 lanes
- CrystalFree™ technology; no external clock reference
- Supports full and fast link training, and no link training
- 18/24/30 RGB color format input
- 18/24 bit panel interface with FRC, ACC and gamma
- Internal color engine
- Programmable BIST and aging patterns
- Autonomous dynamic backlight control capability
- Supports DisplayPort™ standard SSC 0.5% down spreading
- Programmable panel-side clock spreading
- Supports multiple panel-side interface standards
- Supports eDP DRR/nvDPS/sDRRS power saving modes
- Full eDP display authentication support including ASSR
- ESD HBM 8kV
- Low power consumption, optimized for mobile platforms
- 5x12mm vBGA package

### GENERAL DESCRIPTION

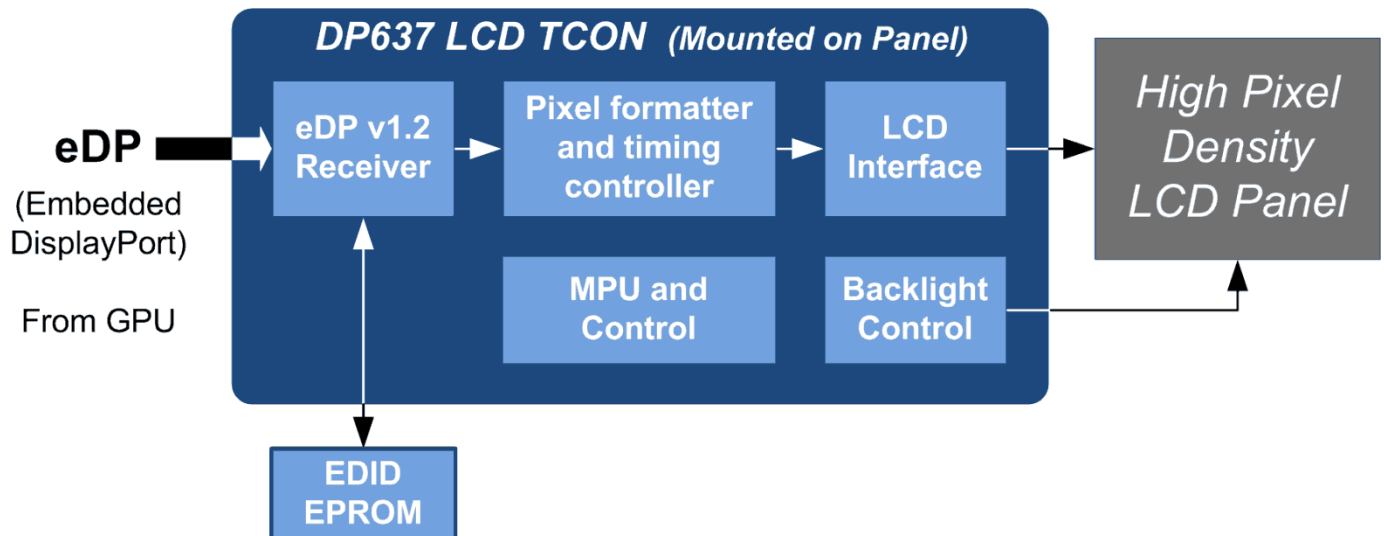
The DP637 is designed for high pixel density LCD panels for use in mobile applications. It leverages the VESA Embedded DisplayPort (eDP) standard that supports a high data rate across a reduced wire-count interface, making it ideal for high pixel density mobile display applications.

The device supports panel resolutions exceeding 2560x1600, which translates to 215 pixels-per-inch on a 14 inch display, providing an image which is better than Full HD.

The DP637 provides a high level of integration for the LCD panel vendor. No external crystal clock reference is needed, and with firmware-less operation, no external memory is needed other than an EEPROM for EDID and initialization. An internal MPU with SPI interface is available for optional use. Using 1, 2, or 4 eDP data lanes, resolutions from VGA (640x480) to WQXGA (2560x1600) can be supported.

### APPLICATIONS

- High Resolution LCD Panels for Mobile PC platforms



Rev.0

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