Parade Technologies

LCD TIMING CONTROLLER WITH DISPLAYPORT RECEIVER

DP621

KEY FEATURES

- DisplayPort Receiver compliant with DisplayPort Specification 1.1a for both 1.62 and 2.7 Gbps
- Very low power consumption, 255mW to 430mW to support up to WUXGA
- No crystal or external reference clock needed with CrystalFree technology
- Built-in adaptive equalization to support 2.7 Gbps transmission over minimal 15m AWG28 cable without requesting transmitter pre-emphasis
- Excellent ESD performances; HBM 8kV at connector pins and 5kV all other pins
- Support DisplayPort 1 or 2 lanes operation
- Support additional Spread Spectrum Clocking on DisplayPort Receiver, RSDS/mini-LVDS transmitter to reduce EMI
- Support 18/24-bit RGB color format
- HDCP 1.3 for Content Protection, Integrated HDCP key ROM
- On-chip microprocessor with SPI ROM interface
- Support various LCD panels including WUXGA (1920x1200), UXGA (1600x1200), WSXGA+ (1680x1050), SXGA+ (1440x1050), SXGA (1280x1024), WXGA+ (1440x900) and WXGA (1280x800, or 1360x768, or 1280x768)
- Support reduced blanking, reduced refresh rate and dynamic refresh rate timing mode
- Programmable TCON control signals generation and programmable FRC patterns
- 6-bit, single RSDS or dual RSDS output, maximum clock rate of 90MHz (for WUXGA)
- 6 or 8-bit, dual mini-LVDS output, maximum clock rate of 162MHz (for WUXGA)
- Support asymmetrical configuration with 3:4 left-right ratio in the number of column drivers by selecting output clock frequency from the video clock frequency of 5, 10, 15, 25%
- Support main link and RSDS/mini-LVDS pin swapping for top or bottom mounting PCBs
- LCD power sequence control
- Support fail-safe mode by scaling to VGA (640x480, 60Hz)
- Support programmable video pattern generation
- Light sensor input and programmable Pulse-Width-Modulation backlight control output
- Low bandwidth ADC for up to 16-button inputs
- Slave I2C interface for chip control
- I2C masters for expansion function
- 100-pin TQFP RoHS Package

APPLICATIONS

- Direct Drive LCD Monitor
- Notebook LCD panels
- Embedded LCD panels

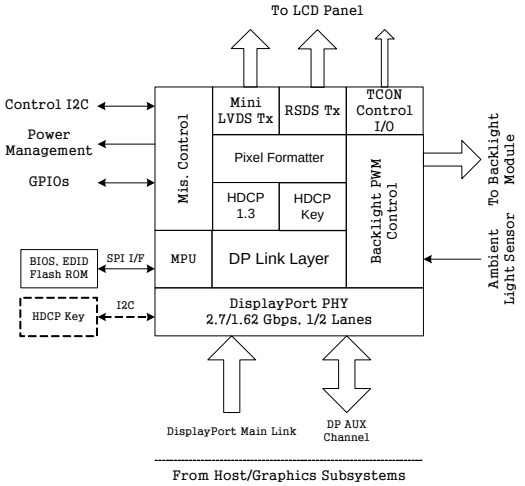
GENERAL DESCRIPTION

The DisplayPort display interface specification leverages matured technologies such as physical layer of PCI Express, packet based transaction and quality of service of data communication, and advanced CMOS semiconductor process to address existing and future growth of digital display on PC and consumer electronics applications. DP621, an LCD Timing controller with DisplayPort Receiver, provides a scalable and interoperable digital display interface together with a programmable timing control scheme to address broad applications on PC and embedded display devices.

DP621 accepts 18/24-bit RGB formats from DisplayPort transmitter devices. DP621 combines a DisplayPort receiver core, which deserializes, un-packs incoming bit stream, with an LCD timing controller (TCON), together with RSDS/mini-LVDS interfaces to support LCD panels for Direct Driver Monitor (DDM) applications.

DP621 supports source device hot plug/unplug detection by sensing voltage levels at AUX channel. It receives command and report configuration and status of main link services through AUX channel.

FUNCTIONAL BLOCK DIAGRAM



Rev.0

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