Parade Technologies

DISPLAYPORT LCD TIMING CONTROLLER FOR EMBEDDED SYSTEMS

DP603

KEY FEATURES

- DisplayPort 1.1a compliant receiver, supporting 1 or 2 lanes width, and 2.7Gbps or 1.62Gbps link rate.
- Low power consumption, 236mW for WXGA+ (1440x900)
- No crystal or external reference clock needed with CrystalFree technology
- Adaptive or programmable equalization to remove any DisplayPort TX pre-emphasis request to lower system power
- Support reduced RSDS/min-LVDS swing to save power
- Support no hand shaking DisplayPort connection
- High receiving sensitivity allowing DP TX 200mVpp swing to minimize system power
- Excellent ESD performances; HBM 5kV
- Support additional Spread Spectrum Clocking on DisplayPort Receiver, RSDS/mini-LVDS transmitter to reduce EMI
- Support 18/24-bit RGB color format
- On-chip microprocessor with SPI ROM interface
- Support various LCD panels including WUXGA (1920x1200), UXGA (1600x1200), WSXGA+ (1680x1050), SXGA+ (1440x1050), SXGA (1280x1024), WXGA+ (1440x900) and WXGA (1280x800, or 1360x768, or 1280x768)
- Support reduced blanking, reduced refresh rate and dynamic refresh rate timing mode
- Programmable TCON control signals generation and programmable FRC patterns
- 6-bit, single RSDS or dual RSDS output
- 6 or 8-bit, dual mini-LVDS output
- Support asymmetrical configuration with 3:4 left-right ratio in the number of column drivers
- Support main link and RSDS/mini-LVDS pin swapping for top or bottom mounting PCBs
- LCD power sequence control
- Support programmable video pattern generation
- Light sensor input and programmable Pulse-Width-Modulation backlight control output
- Slave I2C interface for chip control
- I2C masters for expansion function
- 100-pin TQFP RoHS Package

APPLICATIONS

- Direct Drive LCD Monitor
- Notebook LCD panels
- Embedded LCD panels

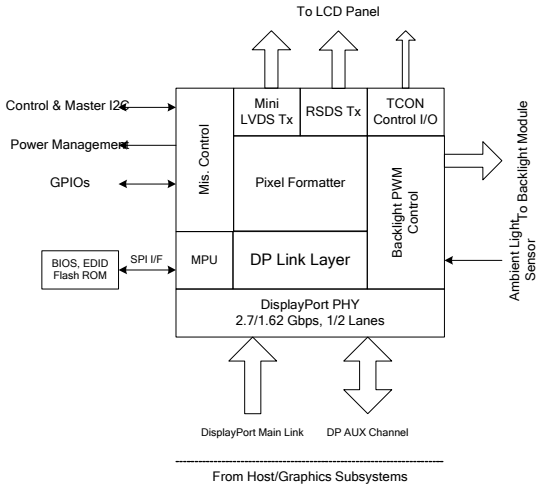
GENERAL DESCRIPTION

The DisplayPort display interface specification leverages matured technologies such as physical layer of PCI Express, packet based transaction and quality of service of data communication, and advanced CMOS semiconductor process to address existing and future growth of digital display on PC and consumer electronics applications. DP603, an LCD Timing controller with DisplayPort Receiver, provides a scalable and interoperable digital display interface together with a programmable timing control scheme to address the embedded display applications.

DP603 accepts 18/24-bit RGB formats from DisplayPort transmitter devices. DP603 combines a DisplayPort receiver core, which deserializes, un-packs incoming bit stream, with an LCD timing controller (TCON), together with RSDS/mini-LVDS interfaces to support LCD panels for embedded applications.

When DP603 is used in embedded LCD display, it can be configured to either using native AUX channel to read EDID and to support DisplayPort hand shaking communications or using I2C to read EDID and to establish DisplayPort connection without hand shaking training. When it is used with AUX channel, DisplayPort command and status of the link services can be communicated between Source and Sink through AUX channel.

FUNCTIONAL BLOCK DIAGRAM



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